EXAMINER'S AMENDMENT

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Hidenobu FUKUMASA Appl. No. 09/914,009 Response to Office Action dated June 8, 2005

a mapping circuit disposed prior to the transmitter for mapping data input thereto to points on the I-Q plane.

Claim 5 (Previously Presented): A spread spectrum communication system including a transmitter and receiver for performing spread spectrum communications based on a direct sequence spreading scheme,

the transmitter comprising:

a permuting processor for permuting an I-phase component signal and a Q-phase component signal of a transmission signal once every two clock units and, at the same time, inverting the sign of one of the I-phase and Q-phase component signals;

a multiplier for multiplying signals output from the permuting processor by a pseudorandom sequence which is generated at a speed exceeding a symbol rate of the transmission signal;

a roll-off filter for waveform shaping; and

a carrier modulator for performing carrier modulation of signals having undergone waveform shaping,

the receiver comprising:

a carrier demodulator for performing carrier demodulation of a received signal; and a multiplier for multiplying two types of signals output from the carrier demodulator by the pseudo-random sequence;

a permuting processor for permuting a signal corresponding to the I-phase component signal multiplied by the pseudo-random sequence once every two clock units and, at the same time, inverting the sign of a signal corresponding to the component signal which underwent sign inversion at the transmitter; and

a phase-correcting portion-for-performing phase-correction-so-as-to-extract-the-I-phase-and-Q-phase-component-signals.

Claim 6 (Previously Presented): The spectrum spread communication system according to Claim 5, wherein the permuting processor of the transmitter includes:

a multiplier for multiplying one of the component signals of the transmission signal by

-1; and

a switch which, based on a control signal of 1 and 0 appearing alternately, switches between a combination of the I-phase component signal and the Q-phase component signal of the transmission signal and a combination of the one component signal multiplied by -1 and the other component signal, •

the permuting processor of the receiver includes:

a multiplier for multiplying the signal which was multiplied by the pseudo-random sequence by -1;

a switch which, based on a control signal of 1 and 0 appearing alternately, switches between a combination of the signals which were multiplied by the pseudo-random sequence and a combination of the one signal multiplied by —1 and the other signal multiplied by the pseudo-random sequence.

Claim 7 (Previously Presented): The spectrum spread communication system according to Claim 5, further comprising:

a mapping circuit disposed prior to the transmitter for mapping data input thereto to points on the I-Q plane.